PATENT ABSTRACTS OF JAPAN

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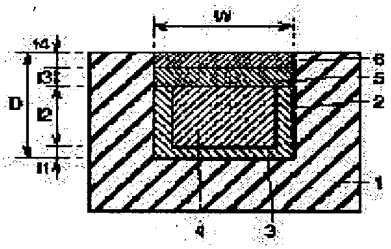
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To suppress the release of a Cu wiring layer from surface by a method, wherein a trench is formed in an insulating layer to interpose an underneath layer in the trench for burying a Cu wiring layer to form a bonding layer covering the wiring layer further forming a cap layer covering the bonding layer.
SOLUTION: A trench 2 is formed in an insulating layer 1, made of silicon oxide film, etc., to form an underneath layer 3 made of TiN, etc., in the trench 2 further forming a Cu wiring layer 4 on the underneath layer 3. Next, a bonding layer 5 covering the Cu wiring layer 4 and the underneath layer 3 for increasing the bonding strength between a cap layer 6 and the Cu wiring layer 4 is formed. At this time, the bonding layer 5 is to be made of a material for the bonding strength between the bonding layer 5 and the Cu wiring layer 4 to exceed that between the Cu wiring 4 and the cap layer 6 as well as the growing rate of an oxide not exceeding that of the Cu wiring 4. Through these procedures, the connecting strength between the Cu wiring layer 4 and the cap layer 6 can be increased, also enabling the oxidation of the surface of the Cu wiring layer 4 to be suppressed effectively.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device equipped with the insulating layer in which the trench was formed, the wiring layer constituted by the quality of the material which is intervened and embedded in a substrate layer in said trench, and contains Cu, the adhesion layer formed in said trench so that said wiring layer might be covered, and the cap layer formed in said trench so that said adhesion layer might be covered.
[Claim 2] Said adhesion layer is a semiconductor device according to claim 1 with which adhesion reinforcement with said wiring layer is constituted by the quality of the material larger [than the adhesion reinforcement of said wiring layer and said cap layer] and smaller than it [in / in the growth rate of an oxide / said wiring layer].
[Claim 3] The semiconductor device according to claim 1 or 2 which formed the reaction layer by making said adhesion layer and said wiring layer react between said cap layers and said wiring layers.
[Claim 4] The semiconductor device according to claim 3 from which said all adhesion layers located on said wiring layer were changed into said reaction layer.
[Claim 5] It has the insulating layer in which the trench was formed, and the wiring layer constituted by the quality of the material which is intervened and embedded in a substrate layer in said trench, and contains Cu. In the side-attachment-wall upper limit corner section of said trench It is the semiconductor device with which the periphery section of said cap layer extends on the side-attachment-wall upper limit corner section of said trench rounded off by performing processing which rounds off said corner section by performing processing which rounds off this corner section, and forming a cap layer in said trench so that said wiring layer may be covered.
[Claim 6] The side-attachment-wall upper limit corner section of said trench is a semiconductor device according to claim 5 constituted by the curved surface which has the radius of curvature of 2-20nm.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention is embedded in the trench formed in the insulating layer about a semiconductor device, and relates to the semiconductor device which has the wiring layer constituted by the quality of the material containing Cu.
[0002]
[Description of the Prior Art] Since the demand to high integration and improvement in the speed of a semiconductor device is increasing increasingly and it corresponds to such high integration and improvement in the speed, various examination also about a wiring material is made. Especially, about 0.15 micrometers of wiring width of face are considered that a thing usable as a wiring material is limited extremely in subsequent generations. In such an ingredient, using Cu as a wiring material in recent years is proposed.
[0003] An example of the wiring structure in the case of using Cu as a wiring material is shown in drawing 14 . The wiring structure shown in this drawing 14 is formed of the wiring process using the method called the so-called "DAMASHIN method." The DAMASHIN method is indicated by monthly publication Semiconductor World 1995.12 "the wiring process using a DAMASHIN method" etc., for example.
[0004] As shown in drawing 14 , the trench 2 is formed in the insulating layer 1, in this trench 2, the substrate layer 3 is intervened and the Cu wiring layer 4 is formed. The cap layer 6 is formed so that the top face of this Cu wiring layer 4 may be covered. This cap layer 6 is constituted by TiWN etc. and has the function which controls oxidation of the top face of the Cu wiring layer 4. By having such a cap layer 6, oxidation of the top face of the Cu wiring layer 4 becomes possible [it being controlled effectively and controlling effectively property degradation of a resistance rise of the Cu wiring layer 4 etc.].
[0005] Thus, forming the cap layer 6 is indicated by Shingaku Giho TECHNICAL REPORT OF IEICE.SDM 96-169 (1996-12) "DAMASHIN Cu wiring capped by TiWN" etc., for example.
[0006] Next, the manufacture approach of the wiring structure shown in drawing 14 is explained using drawing 15 - drawing 18 . Drawing 15 - drawing 18 are the sectional views showing the 1st process of the production process of the wiring structure shown in drawing 14 - the 4th process.

[0007] With reference to drawing 15 , a trench 2 is formed in an insulating layer 1 using a photoengraving-process technique, an etching technique, etc. next, it is shown in drawing 16 -- as -- CVD (Chemical Vapor Deposition) -- TiN layer 3a is formed using law etc., on this TiN layer 3a, the sputtering method etc. is used and Cu layer 4a is formed.
[0008] Next, CMP (Chemical Mechanical Polishing) processing is performed to the above-mentioned Cu layer 4a and TiN layer 3a. Thereby, while exposing the front face of an insulating layer 1, it leaves Cu layer only in a trench 2. Consequently, as shown in drawing 17 , the substrate layer 3 and the Cu wiring layer 4 are formed in a trench 2, respectively.
[0009] Next, as shown in drawing 18 , TiWN layer 6a is formed using the sputtering method etc. And CMP processing is performed to this TiWN layer 6a. The wiring structure shown in drawing 14 will be acquired through the above process.

[0010]
[Problem(s) to be Solved by the Invention] Although it became possible to control oxidation of the top face of the Cu wiring layer 4 by forming cap layer 6a as mentioned above, when the wiring structure by which the artificer of this application is shown in drawing 14 was made as an experiment, it checked that exfoliation may arise in the interface of the above-mentioned cap layer 6 and the Cu wiring layer 4. As one factor of this exfoliation, it is possible that the adhesion reinforcement of the Cu wiring layer 4 and the cap layer 6 is weak. Moreover, the artificer of this application also checked that it was easy to produce the above-mentioned exfoliation in the periphery section of the cap layer 6. From this, a certain stress concentrates in the periphery section of the cap layer 6, and it is thought that this stress concentration can also serve as a cause of the above-mentioned exfoliation.
[0011] When the above exfoliations arise in the interface of the cap layer 6 and the Cu wiring layer 4, the top face of the Cu wiring layer 4 oxidizes, and we are anxious about property degradation of a resistance rise of the Cu wiring layer 4 etc. And the fall of the yield and the fall of a wiring life will be caused by such property degradation of the Cu wiring layer 4.
[0012] This invention is made in order to solve the above technical problems. The purpose of this invention is to control the exfoliation from the front face of the Cu wiring layer 4.
[0013]
[Means for Solving the Problem] The semiconductor device concerning this invention is equipped with an insulating layer, a wiring layer, an adhesion layer, and a cap layer on one aspect of affairs. A trench is formed in an insulating layer, a substrate layer is intervened in this trench, and a wiring layer is embedded. This wiring layer is constituted by the quality of the material containing Cu. An adhesion layer is formed in a trench so that a wiring layer may be covered, and a cap layer is formed in a trench so that an adhesion layer may be covered. Here, the above-mentioned substrate layer has the diffusion prevention function of the wiring layer ingredient to the inside of an insulating layer, and a function as an adhesion layer of a wiring layer and an insulating layer. Moreover, an adhesion layer has large adhesion reinforcement with the both sides of a wiring layer and a cap layer, and it has the function to connect both firmly. Moreover, a cap layer has oxidation resistance and has the function which controls that a wiring layer oxidizes.
[0014] In addition, it is constituted by the quality of the material with adhesion reinforcement preferably larger [the above-mentioned adhesion layer] than the adhesion reinforcement of a wiring layer and a cap layer and with a cap layer, and the growth rate of an oxide smaller than it in a wiring layer.
[0015] Moreover, it is desirable to form a reaction layer by making an adhesion layer and a wiring layer react between the above-mentioned cap layer and a wiring layer.
[0016] Moreover, when forming a reaction layer as mentioned above, all the adhesion layers located on a wiring layer may be changed into a reaction layer.
[0017] The semiconductor device concerning this invention is equipped with an insulating layer, a wiring layer, and a cap layer on other aspects of affairs. A trench is formed in an insulating layer, a substrate layer is intervened in this trench, and a wiring layer is embedded. This wiring layer is constituted by the quality of the material containing Cu. A cap layer is formed in a trench so that a wiring layer may be covered. And processing which rounds off this corner section is performed to the side-attachment-wall upper limit corner section of a trench. For example, when the above-mentioned insulating layer is constituted by silicon oxide, light etching processing in which the fluoric acid system was used for the insulating layer after the trench was formed is performed. By performing such processing, the trench side-attachment-wall upper limit corner section is rounded off, and the periphery section of the above-mentioned cap layer extends on the side-attachment-wall upper limit corner section of this trench rounded off.
[0018] In addition, as for the side-attachment-wall upper limit corner section of the above-mentioned trench, it is desirable to be constituted by the curved surface which has the radius of curvature of 2-20nm. At this time, as long as it is a thing within the limits of 2-20nm as mentioned above, the side-attachment-wall upper limit corner section of a trench may be constituted by putting in a row the curved surface which has different radius of curvature.

[0019]
[Embodiment of the Invention] Hereafter, the gestalt of implementation of this invention is explained using drawing 1 - drawing 11 .
[0020] (Gestalt 1 of operation) The gestalt 1 of implementation of this invention is first explained using drawing 1 - drawing 7 . Drawing 1 is the sectional view showing the wiring structure in the gestalt 1 of implementation of this invention.
[0021] The trench 2 is formed in the insulating layer 1 which consists of silicon oxide etc. with reference to drawing 1 . The aperture width W of a trench 2 is about 0.18 micrometers, and depth D of a trench 2 is about 0.3 micrometers. In addition, the aspect ratio of a trench 2 may be one to about 1.5.
[0022] In a trench 2, the substrate layer 3 which consists of TiN etc. is formed. The thickness t1 of this substrate layer 3 is about 10nm. The Cu wiring layer 4 is formed on this substrate layer 3. The thickness t2 of this Cu wiring layer 4 is about 200nm. In addition, it is also possible to use CuZr, CuTi, CuAl, etc. instead of the Cu wiring layer 4.
[0023] The adhesion layer 5 is formed so that the Cu wiring layer 4 and the substrate layer 3 may be covered. This adhesion layer 5 is formed so that it may raise the adhesion reinforcement of the cap layer 6 and the Cu wiring layer 4 which are formed on the adhesion layer 5, the adhesion reinforcement of the adhesion layer 5 and the Cu wiring layer 4 is larger than the adhesion reinforcement of the Cu wiring layer 4 and the cap layer 6, and it is desirable that the growth rate of an oxide is constituted by the quality of the material smaller than it in the Cu wiring layer 4. While this becomes possible [raising the connection resilience of the Cu wiring layer 4 and the cap layer 6 rather than the conventional example], it becomes possible also about the top face of the Cu wiring layer 4 oxidizing to control effectively.
[0024] As the quality of the material of the above-mentioned adhesion layer 5, Ti, TiN, Cr, aluminum, AlCu, AlSiCu, etc. can be mentioned. Moreover, as for the thickness t3 of this adhesion layer 5, it is desirable that it is about 3-50nm. By considering as such thickness, the above effectiveness is expectable.
[0025] If the cap layer 6 is this case, it is constituted by TiWN. As shown in drawing 1 , this cap layer 6 is embedded in a trench 2 so that the adhesion layer 5 may be covered. Moreover, the thickness t4 of this cap layer 6 is 30nm - about 77nm. By considering as such thickness, it becomes possible to secure the oxidation resistance of the cap layer 6.
[0026] By forming the above adhesion layers 5, it is thought that it becomes possible to control exfoliation of the cap layer 6 effectively. That this should be proved, the artificer of this application evaluated whether exfoliation of the cap layer 6 would arise, when the adhesion layer 5 was formed. The evaluation result is shown in Table 1. In addition, the case where Ti layer is formed as an adhesion layer 5 is shown by Table 1.
[0027]
[Table 1]

構造	CMP 時の TiWN 層に対するストレス	
	ストレス大(研磨レート大:約 400nm/min.)	ストレス小(研磨レート小:約 100nm/min.)
TiN/Cu/TiWN	配線エッジ部から剥離	配線エッジ部で部分的な剥離有り
TiN/Cu/Ti/TiWN	剥離無し	剥離無し
TiN/Cu/Ti/TiWN(熱処理有り)	剥離無し	剥離無し

[0028] As shown in Table 1, when Ti layer which functions as an adhesion layer 5 is formed, it turns out that exfoliation has not arisen irrespective of the size of the stress to the cap layer after CMP (TiWN layer). From this, it is thought by forming the adhesion layer 5 that it becomes possible to control exfoliation of the cap layer 6 effectively. In addition, also when the above-mentioned quality of the materials other than Ti layer are used as an adhesion layer 5, it is imagined as that from which the same result is obtained. Moreover, although what heat-treated after forming the adhesion layer 5 in Table 1 is indicated, about this, it mentions later.
[0029] Next, the manufacture approach of the wiring structure shown in drawing 1 is explained using drawing 2 - drawing 6 . Drawing 2 - drawing 6 are the sectional views showing the 1st

process of the production process of the wiring structure shown in drawing 1 - the 5th process.
[0030] With reference to drawing 2 , a trench 2 is formed using a photoengraving-process technique and a dry etching technique. It is as having mentioned above about the dimension of this trench 2.
[0031] Next, for example using a CVD method etc., TiN layer 3a is formed in the thickness of about 10nm so that it may extend on an insulating layer 1 from the inside of a trench 2. On this TiN layer 3a, a CVD method or the sputtering method is used and Cu layer 4a with a thickness of about 400nm is formed.
[0032] Next, CMP processing is performed to the above-mentioned Cu layer 4a and TiN layer 3a. This CMP processing may be performed using the slurry of for example, the alumina base. And CMP processing is performed until the main front face of an insulating layer 1 is exposed. Consequently, as shown in drawing 4 , while the Cu wiring layer 4 and the substrate layer 3 are formed, the recess section 7 is formed on these. The depth D1 of this recess section 7 is selected so that it may become the sum of the thickness of the adhesion layer 5 and the cap layer 6 which are formed at a next process, and if it is this case, it is about 80nm, for example. In addition, as for the depth D1 of the recess section 7, it is desirable to be set as about 50-80nm and a comparatively small value. Thereby, reduction of the cross section of the Cu wiring layer 4 can be controlled, and the rise of wiring resistance can be controlled.
[0033] Next, as shown in drawing 5 , Ti layer 5a is formed in the thickness of about 200nm using the sputtering method etc. And CMP processing is performed to this Ti layer 5a.
[0034] This becomes possible to form the adhesion layer 5 so that it may be embedded in a trench 2, as shown in drawing 6 . Then, TiWN layer 6a is further formed in the thickness of about 200nm using the sputtering method etc. And CMP processing is performed also to this TiWN layer 6a. Also in this case, CMP processing using the slurry of the alumina base may be performed. The wiring structure shown in drawing 1 will be acquired through the above process.
[0035] In addition, sequential formation of the above-mentioned Ti layer 5a and the TiWN layer 6a may be carried out, and CMP processing may be performed to these laminated structures.
[0036] Next, the example of application of the wiring structure in the gestalt 1 of this operation is explained using drawing 7 . Drawing 7 is the sectional view showing an example of the semiconductor device with which the wiring structure in the gestalt 1 of the above-mentioned operation was applied. Specifically, a part of DRAM (Dynamic Random Access Memory) to which the wiring structure of the gestalt 1 of the above-mentioned operation was applied is shown in drawing 7 .
[0037] With reference to drawing 7 , the impurity diffusion fields 14a and 14b are formed in the main front face of a silicon substrate 10 so that a channel field may be specified. Trenches 11a and 11b are formed in the both sides of these impurity diffusion fields 14a and 14b. In trench 11a and 11b, insulating layers 12a and 12b are intervened, and the polish recon layers 13a and 13b are formed, respectively.
[0038] The gate insulating layer 15 is intervened on the above-mentioned channel field, and the gate electrode 16 is formed. On the main front face of a silicon substrate 10, layer insulation layer 18a which consists of a silicon oxide etc. is formed so that this gate electrode 16 may be covered. Contact holes 11c and 11d are formed in this layer insulation layer 18a so that it may arrive at the impurity diffusion fields 14a and 14b. In contact hole 11c and 11d, the plug electrodes 17a and 17b which consist of W etc. are formed.
[0039] Layer insulation layer 18b is formed so that layer insulation layer 18a may be covered. A trench 23 is formed in this layer insulation layer 18b, and the substrate layer 19 which consists of TiN etc. is formed in this trench 23. The Cu wiring layer 20 is formed on this substrate layer 19, and the adhesion layer 21 is formed on this Cu wiring layer 20. And on this adhesion layer 21, the cap layer 22 which consists of TiWN is formed. On layer insulation layer 18b, layer insulation layer 18c is formed so that the cap layer 22 may be covered. In addition, although Cu wiring layer may be formed also in this layer insulation layer 18c, that illustration and explanation are omitted.

[0040] (Gestalt 2 of operation) Next, the gestalt 2 of implementation of this invention is explained using drawing 8 and drawing 9 . Drawing 8 is the sectional view showing the wiring

structure in the gestalt 2 of implementation of this invention. Drawing 9 is the sectional view showing the modification of the wiring structure shown in drawing 8 .
[0041] With reference to drawing 8 , the reaction layer 8 is formed between the adhesion layer 5 and the Cu wiring layer 4 with the gestalt 2 of this operation. In this reaction layer 8, it is the layer formed of the counter diffusion of the element which constitutes the Cu wiring layer 4 and the adhesion layer 5, and it becomes possible by forming such a reaction layer 8 to raise the connection resilience of the adhesion layer 5 and the Cu wiring layer 4 further from the case of the gestalt 1 of the above-mentioned operation. Consequently, it becomes possible from the case of the gestalt 1 of operation of the above [exfoliation of the cap layer 6] to control still more effectively.
[0042] As the formation approach of the above-mentioned reaction layer 8, when the adhesion layer 5 is constituted by Ti, it is 200 degrees C - about 400 degrees C in temperature, and can form by performing heat treatment for about 30 minutes within a vacuum or an inert gas ambient atmosphere.
[0043] Next, the modification of the wiring structure shown in drawing 8 is explained using drawing 9 . With reference to drawing 9 , the adhesion layer 5 located on the Cu wiring layer 4 is altogether changed into the reaction layer 8 in this modification by the above-mentioned heat treatment performed after forming the adhesion layer 5. Also in this case, it becomes possible from the case of the gestalt 1 of operation as well as the above-mentioned case to control exfoliation of the cap layer 6 still more effectively. In addition, in this modification, since it is necessary to change altogether into the reaction layer 8 the adhesion layer 5 located on the Cu wiring layer 4, the suitable heat treatment conditions according to the thickness of the adhesion layer 5 are chosen.
[0044] (Gestalt 3 of operation) Next, the gestalt 3 and modification of implementation of this invention are explained using drawing 10 - drawing 13 . Drawing 10 is the sectional view showing the wiring structure in the gestalt 3 of implementation of this invention.
[0045] With reference to drawing 10 , with the gestalt 3 of this operation, side-attachment-wall upper limit corner section 2a of a trench 2 is rounded off, and the cap layer 6 is formed so that it may extend on side-attachment-wall upper limit corner section 2a of such a trench 2 rounded off. As already pointed out as a trouble of the conventional example, the observation result of being easy to produce exfoliation in the periphery section of the cap layer 6 is obtained, and it is guessed that it is what a certain stress concentration tends to produce from this in the periphery section of the cap layer 6.
[0046] Then, the artificer of this application rounds off side-attachment-wall upper limit corner section 2a of a trench 2, and was made to make the periphery section of the cap layer 6 extend on this that the stress concentration in the periphery section of the cap layer 6 should be eased, as shown in drawing 10 . Thereby, the touch area of the periphery section of the cap layer 6 and an insulating layer 1 can be increased conventionally, and it is thought that it enables this to ease stress concentration. Consequently, it is thought that it becomes possible to control effectively exfoliation of the cap layer 6 which had become a problem in the conventional example.
[0047] Next, the manufacture approach of the wiring structure in the gestalt 3 of this operation is explained using drawing 11 - drawing 12 . Drawing 11 - drawing 12 are the sectional views showing the 1st process of the production process of the wiring structure in the gestalt 3 of this operation - the 2nd process.
[0048] After forming a trench 2 with reference to drawing 11 (a) through the same process as the case of the gestalt 1 of the above-mentioned operation, processing which rounds off side-attachment-wall upper limit corner section 2a of a trench 2 is performed. For example, when an insulating layer 1 is silicon oxide, light etching which used the fluoric acid system is performed. Thereby, side-attachment-wall upper limit corner section 2a of a trench 2 is rounded off according to an edge effect.
[0049] Although the enlarged drawing of side-attachment-wall upper limit corner section 2a of a trench 2 is shown in drawing 11 (b), as for side-attachment-wall upper limit corner section 2a, it is desirable to be constituted by the curved surface which has the predetermined radius of

curvature r. And as for this radius of curvature r, it is desirable that it is about 2-20nm. That is because it is thought that spacing during adjoining wiring becomes large and trouble is caused to detailed-ization when it becomes difficult [implementation] very [radius of curvature r] when smaller than 2nm, and radius of curvature r exceeds 20nm. From this, in the range whose radius of curvature r is 2-20nm, it can realize and it is thought that it does not become a problem mostly even if it faces detailed-ization.

[0050] In addition, although the case where the above-mentioned corner section 2a was constituted by the curved surface which has the fixed radius of curvature r was shown in drawing 11 (b), the curved surface which has different radius of curvature r may be put in a row. Moreover, if it sees microscopically, even if it cannot say that it is constituted by the curved surface, what sees on the whole and can be recognized as a curved surface is contained in the concept of the above-mentioned "curved surface."

[0051] Next, with reference to drawing 12 , the Cu wiring layer 4 and the substrate layer 3 are formed by the same approach as the case of the gestalt 1 of the above-mentioned operation, on these, the sputtering method etc. is used and TiWN layer 6a with a thickness of about 200nm is formed. And CMP processing is performed to TiWN layer 6a like the case of the gestalt 1 of the above-mentioned operation. This becomes possible to form the cap layer 6 in a trench 2, so that it may extend on side-attachment-wall upper limit corner section 2a of a trench 2, as shown in drawing 10 .

[0052] Next, the modification of the gestalt 3 of this operation is explained using drawing 13 . As shown in drawing 13 , in this modification, the adhesion layer 5 is formed between the cap layer 6 and the Cu wiring layer 4. It is thought that this becomes possible [controlling exfoliation of the cap layer 6 further] from the case of the gestalt 1 of the above-mentioned operation. In addition, also in this modification, a reaction layer 8 like [in the case of the gestalt 2 of the above-mentioned operation] may be formed.

[0053] As mentioned above, although the gestalt of implementation of this invention was explained, it should be thought that the gestalt of the operation indicated this time is [no] instantiation at points, and restrictive. The range of this invention is shown by the claim and it is meant that all modification in a claim, equal semantics, and within the limits is included.

[0054]

[Effect of the Invention] As explained above, on one aspect of affairs of the semiconductor device concerning this invention, an adhesion layer is formed on a wiring layer and a cap layer is formed on this adhesion layer. Since the quality of the material with large adhesion reinforcement with a cap layer and a wiring layer is chosen as an adhesion layer, it becomes possible to control exfoliation of a cap layer effectively by existence of an adhesion layer. It becomes possible about originating in exfoliation of a cap layer and the top face of a wiring layer oxidizing by that cause, to control effectively, and it becomes possible to control generating of a wiring defect effectively. Consequently, while becoming possible to raise the yield conventionally, it becomes possible to also raise a wiring life.

[0055] In addition, when the above-mentioned adhesion layer is constituted by the quality of the material smaller than it [in / the adhesion reinforcement of this adhesion layer and a wiring layer is larger than the adhesion reinforcement of a wiring layer and a cap layer, and / in the growth rate of an oxide / a wiring layer], it becomes possible it not only can to control exfoliation of a cap layer effectively, but to control that the top face of a wiring layer oxidizes by existence of this adhesion layer.

[0056] Moreover, when the reaction layer by making an adhesion layer and a wiring layer react is formed between a cap layer and a wiring layer, it becomes possible from this reaction layer being formed of the counter diffusion of the ingredient of a wiring layer, and the ingredient of an adhesion layer to control exfoliation of a cap layer still more effectively than the above-mentioned case.

[0057] Moreover, all the above-mentioned adhesion layers may be changed into a reaction layer, and it becomes possible to control exfoliation of a cap layer effectively like the case where a reaction layer is formed between an adhesion layer and a wiring layer, also in this case.

[0058] On other aspects of affairs of the semiconductor device concerning this invention, the

side-attachment-wall upper limit corner section of the trench formed in the insulating layer is rounded off. And the cap layer is made to extend on the side-attachment-wall upper limit corner section rounded off in this way. Thereby, it becomes possible to increase the touch area of the periphery section of a cap layer, and an insulating layer conventionally. The stress concentration in the periphery section of the cap layer about which we were anxious in the conventional example can be eased by that cause, and it becomes possible to control exfoliation of a cap layer rather than the conventional example.

[0059] In addition, as for the above-mentioned side-attachment-wall upper limit corner section, it is desirable to be constituted by the curved surface which has the radius of curvature of about 2-20nm, and the effectiveness of not causing trouble even if it can realize easily and faces detailed-ization of a semiconductor device is acquired by making radius of curvature into such within the limits.

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TECHNICAL FIELD

[Field of the Invention] Especially this invention is embedded in the trench formed in the insulating layer about a semiconductor device, and relates to the semiconductor device which has the wiring layer constituted by the quality of the material containing Cu.

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PRIOR ART

[Description of the Prior Art] Since the demand to high integration and improvement in the speed of a semiconductor device is increasing increasingly and it corresponds to such high integration and improvement in the speed, various examination also about a wiring material is made. Especially, about 0.15 micrometers of wiring width of face are considered that a thing usable as a wiring material is limited extremely in subsequent generations. In such an ingredient, using Cu as a wiring material in recent years is proposed.
[0003] An example of the wiring structure in the case of using Cu as a wiring material is shown in drawing 14 . The wiring structure shown in this drawing 14 is formed of the wiring process using the method called the so-called "DAMASHIN method." The DAMASHIN method is indicated by monthly publication Semiconductor World 1995.12 "the wiring process using a DAMASHIN method" etc., for example.
[0004] As shown in drawing 14 , the trench 2 is formed in the insulating layer 1, in this trench 2, the substrate layer 3 is intervened and the Cu wiring layer 4 is formed. The cap layer 6 is formed so that the top face of this Cu wiring layer 4 may be covered. This cap layer 6 is constituted by TiWN etc. and has the function which controls oxidation of the top face of the Cu wiring layer 4. By having such a cap layer 6, oxidation of the top face of the Cu wiring layer 4 becomes possible [it being controlled effectively and controlling effectively property degradation of a resistance rise of the Cu wiring layer 4 etc.].
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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, on one aspect of affairs of the semiconductor device concerning this invention, an adhesion layer is formed on a wiring layer and a cap layer is formed on this adhesion layer. Since the quality of the material with large adhesion reinforcement with a cap layer and a wiring layer is chosen as an adhesion layer, it becomes possible to control exfoliation of a cap layer effectively by existence of an adhesion layer. It becomes possible about originating in exfoliation of a cap layer and the top face of a wiring layer oxidizing by that cause, to control effectively, and it becomes possible to control generating of a wiring defect effectively. Consequently, while becoming possible to raise the yield conventionally, it becomes possible to also raise a wiring life.
[0055] In addition, when the above-mentioned adhesion layer is constituted by the quality of the material smaller than it [in / the adhesion reinforcement of this adhesion layer and a wiring layer is larger than the adhesion reinforcement of a wiring layer and a cap layer, and / in the growth rate of an oxide / a wiring layer], it becomes possible it not only can to control exfoliation of a cap layer effectively, but to control that the top face of a wiring layer oxidizes by existence of this adhesion layer.
[0056] Moreover, when the reaction layer by making an adhesion layer and a wiring layer react is formed between a cap layer and a wiring layer, it becomes possible from this reaction layer being formed of the counter diffusion of the ingredient of a wiring layer, and the ingredient of an adhesion layer to control exfoliation of a cap layer still more effectively than the above-mentioned case.
[0057] Moreover, all the above-mentioned adhesion layers may be changed into a reaction layer, and it becomes possible to control exfoliation of a cap layer effectively like the case where a reaction layer is formed between an adhesion layer and a wiring layer, also in this case.
[0058] On other aspects of affairs of the semiconductor device concerning this invention, the side-attachment-wall upper limit corner section of the trench formed in the insulating layer is rounded off. And the cap layer is made to extend on the side-attachment-wall upper limit corner section rounded off in this way. Thereby, it becomes possible to increase the touch area of the periphery section of a cap layer, and an insulating layer conventionally. The stress concentration in the periphery section of the cap layer about which we were anxious in the conventional example can be eased by that cause, and it becomes possible to control exfoliation of a cap layer rather than the conventional example.
[0059] In addition, as for the above-mentioned side-attachment-wall upper limit corner section, it is desirable to be constituted by the curved surface which has the radius of curvature of about 2-20nm, and the effectiveness of not causing trouble even if it can realize easily and faces detailed-ization of a semiconductor device is acquired by making radius of curvature into such within the limits.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Although it became possible to control oxidation of the top face of the Cu wiring layer 4 by forming cap layer 6a as mentioned above, when the wiring structure by which the artificer of this application is shown in drawing 14 was made as an experiment, it checked that exfoliation may arise in the interface of the above-mentioned cap layer 6 and the Cu wiring layer 4. As one factor of this exfoliation, it is possible that the adhesion reinforcement of the Cu wiring layer 4 and the cap layer 6 is weak. Moreover, the artificer of this application also checked that it was easy to produce the above-mentioned exfoliation in the periphery section of the cap layer 6. From this, a certain stress concentrates in the periphery section of the cap layer 6, and it is thought that this stress concentration can also serve as a cause of the above-mentioned exfoliation.
[0011] When the above exfoliations arise in the interface of the cap layer 6 and the Cu wiring layer 4, the top face of the Cu wiring layer 4 oxidizes, and we are anxious about property degradation of a resistance rise of the Cu wiring layer 4 etc. And the fall of the yield and the fall of a wiring life will be caused by such property degradation of the Cu wiring layer 4.
[0012] This invention is made in order to solve the above technical problems. The purpose of this invention is to control the exfoliation from the front face of the Cu wiring layer 4.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem] The semiconductor device concerning this invention is equipped with an insulating layer, a wiring layer, an adhesion layer, and a cap layer on one aspect of affairs. A trench is formed in an insulating layer, a substrate layer is intervened in this trench, and a wiring layer is embedded. This wiring layer is constituted by the quality of the material containing Cu. An adhesion layer is formed in a trench so that a wiring layer may be covered, and a cap layer is formed in a trench so that an adhesion layer may be covered. Here, the above-mentioned substrate layer has the diffusion prevention function of the wiring layer ingredient to the inside of an insulating layer, and a function as an adhesion layer of a wiring layer and an insulating layer. Moreover, an adhesion layer has large adhesion reinforcement with the both sides of a wiring layer and a cap layer, and it has the function to connect both firmly. Moreover, a cap layer has oxidation resistance and has the function which controls that a wiring layer oxidizes.
[0014] In addition, it is constituted by the quality of the material with adhesion reinforcement preferably larger [the above-mentioned adhesion layer] than the adhesion reinforcement of a wiring layer and a cap layer and with a cap layer, and the growth rate of an oxide smaller than it in a wiring layer.
[0015] Moreover, it is desirable to form a reaction layer by making an adhesion layer and a wiring layer react between the above-mentioned cap layer and a wiring layer.
[0016] Moreover, when forming a reaction layer as mentioned above, all the adhesion layers located on a wiring layer may be changed into a reaction layer.
[0017] The semiconductor device concerning this invention is equipped with an insulating layer, a wiring layer, and a cap layer on other aspects of affairs. A trench is formed in an insulating layer, a substrate layer is intervened in this trench, and a wiring layer is embedded. This wiring layer is constituted by the quality of the material containing Cu. A cap layer is formed in a trench so that a wiring layer may be covered. And processing which rounds off this corner section is performed to the side-attachment-wall upper limit corner section of a trench. For example, when the above-mentioned insulating layer is constituted by silicon oxide, light etching processing in which the fluoric acid system was used for the insulating layer after the trench was formed is performed. By performing such processing, the trench side-attachment-wall upper limit corner section is rounded off, and the periphery section of the above-mentioned cap layer extends on the side-attachment-wall upper limit corner section of this trench rounded off.
[0018] In addition, as for the side-attachment-wall upper limit corner section of the above-mentioned trench, it is desirable to be constituted by the curved surface which has the radius of curvature of 2-20nm. At this time, as long as it is a thing within the limits of 2-20nm as mentioned above, the side-attachment-wall upper limit corner section of a trench may be constituted by putting in a row the curved surface which has different radius of curvature.
[0019]
[Embodiment of the Invention] Hereafter, the gestalt of implementation of this invention is explained using drawing 1 - drawing 11 .
[0020] (Gestalt 1 of operation) The gestalt 1 of implementation of this invention is first explained using drawing 1 - drawing 7 . Drawing 1 is the sectional view showing the wiring structure in the

gestalt 1 of implementation of this invention.
[0021] The trench 2 is formed in the insulating layer 1 which consists of silicon oxide etc. with reference to drawing 1 . The aperture width W of a trench 2 is about 0.18 micrometers, and depth D of a trench 2 is about 0.3 micrometers. In addition, the aspect ratio of a trench 2 may be one to about 1.5.
[0022] In a trench 2, the substrate layer 3 which consists of TiN etc. is formed. The thickness t1 of this substrate layer 3 is about 10nm. The Cu wiring layer 4 is formed on this substrate layer 3. The thickness t2 of this Cu wiring layer 4 is about 200nm. In addition, it is also possible to use CuZr, CuTi, CuAl, etc. instead of the Cu wiring layer 4.
[0023] The adhesion layer 5 is formed so that the Cu wiring layer 4 and the substrate layer 3 may be covered. This adhesion layer 5 is formed so that it may raise the adhesion reinforcement of the cap layer 6 and the Cu wiring layer 4 which are formed on the adhesion layer 5, the adhesion reinforcement of the adhesion layer 5 and the Cu wiring layer 4 is larger than the adhesion reinforcement of the Cu wiring layer 4 and the cap layer 6, and it is desirable that the growth rate of an oxide is constituted by the quality of the material smaller than it in the Cu wiring layer 4. While this becomes possible [raising the connection resilience of the Cu wiring layer 4 and the cap layer 6 rather than the conventional example], it becomes possible also about the top face of the Cu wiring layer 4 oxidizing to control effectively.
[0024] As the quality of the material of the above-mentioned adhesion layer 5, Ti, TiN, Cr, aluminum, AlCu, AlSiCu, etc. can be mentioned. Moreover, as for the thickness t3 of this adhesion layer 5, it is desirable that it is about 3-50nm. By considering as such thickness, the above effectiveness is expectable.
[0025] If the cap layer 6 is this case, it is constituted by TiWN. As shown in drawing 1 , this cap layer 6 is embedded in a trench 2 so that the adhesion layer 5 may be covered. Moreover, the thickness t4 of this cap layer 6 is 30nm - about 77nm. By considering as such thickness, it becomes possible to secure the oxidation resistance of the cap layer 6.
[0026] By forming the above adhesion layers 5, it is thought that it becomes possible to control exfoliation of the cap layer 6 effectively. That this should be proved, the artificer of this application evaluated whether exfoliation of the cap layer 6 would arise, when the adhesion layer 5 was formed. The evaluation result is shown in Table 1. In addition, the case where Ti layer is formed as an adhesion layer 5 is shown by Table 1.
[0027]
[Table 1]

構造	CMP 時の TiWN 層に対するストレス	
	ストレス大(研磨レート大:約 400nm/min.)	ストレス小(研磨レート小:約 100nm/min.)
TiN/Cu/TiWN	配線エッジ部から剥離	配線エッジ部で部分的な剥離有り
TiN/Cu/Ti/TiWN	剥離無し	剥離無し
TiN/Cu/Ti/TiWN(熱処理有り)	剥離無し	剥離無し

[0028] As shown in Table 1, when Ti layer which functions as an adhesion layer 5 is formed, it turns out that exfoliation has not arisen irrespective of the size of the stress to the cap layer after CMP (TiWN layer). From this, it is thought by forming the adhesion layer 5 that it becomes possible to control exfoliation of the cap layer 6 effectively. In addition, also when the above-mentioned quality of the materials other than Ti layer are used as an adhesion layer 5, it is imagined as that from which the same result is obtained. Moreover, although what heat-treated after forming the adhesion layer 5 in Table 1 is indicated, about this, it mentions later.
[0029] Next, the manufacture approach of the wiring structure shown in drawing 1 is explained using drawing 2 - drawing 6 . Drawing 2 - drawing 6 are the sectional views showing the 1st process of the production process of the wiring structure shown in drawing 1 - the 5th process.
[0030] With reference to drawing 2 , a trench 2 is formed using a photoengraving-process technique and a dry etching technique. It is as having mentioned above about the dimension of this trench 2.
[0031] Next, for example using a CVD method etc., TiN layer 3a is formed in the thickness of

about 10nm so that it may extend on an insulating layer 1 from the inside of a trench 2. On this TiN layer 3a, a CVD method or the sputtering method is used and Cu layer 4a with a thickness of about 400nm is formed.
[0032] Next, CMP processing is performed to the above-mentioned Cu layer 4a and TiN layer 3a. This CMP processing may be performed using the slurry of for example, the alumina base. And CMP processing is performed until the main front face of an insulating layer 1 is exposed. Consequently, as shown in drawing 4 , while the Cu wiring layer 4 and the substrate layer 3 are formed, the recess section 7 is formed on these. The depth D1 of this recess section 7 is selected so that it may become the sum of the thickness of the adhesion layer 5 and the cap layer 6 which are formed at a next process, and if it is this case, it is about 80nm, for example. In addition, as for the depth D1 of the recess section 7, it is desirable to be set as about 50-80nm and a comparatively small value. Thereby, reduction of the cross section of the Cu wiring layer 4 can be controlled, and the rise of wiring resistance can be controlled.
[0033] Next, as shown in drawing 5 , Ti layer 5a is formed in the thickness of about 200nm using the sputtering method etc. And CMP processing is performed to this Ti layer 5a.
[0034] This becomes possible to form the adhesion layer 5 so that it may be embedded in a trench 2, as shown in drawing 6 . Then, TiWN layer 6a is further formed in the thickness of about 200nm using the sputtering method etc. And CMP processing is performed also to this TiWN layer 6a. Also in this case, CMP processing using the slurry of the alumina base may be performed. The wiring structure shown in drawing 1 will be acquired through the above process.
[0035] In addition, sequential formation of the above-mentioned Ti layer 5a and the TiWN layer 6a may be carried out, and CMP processing may be performed to these laminated structures.
[0036] Next, the example of application of the wiring structure in the gestalt 1 of this operation is explained using drawing 7 . Drawing 7 is the sectional view showing an example of the semiconductor device with which the wiring structure in the gestalt 1 of the above-mentioned operation was applied. Specifically, a part of DRAM (Dynamic Random Access Memory) to which the wiring structure of the gestalt 1 of the above-mentioned operation was applied is shown in drawing 7 .
[0037] With reference to drawing 7 , the impurity diffusion fields 14a and 14b are formed in the main front face of a silicon substrate 10 so that a channel field may be specified. Trenches 11a and 11b are formed in the both sides of these impurity diffusion fields 14a and 14b. In trench 11a and 11b, insulating layers 12a and 12b are intervened, and the polish recon layers 13a and 13b are formed, respectively.
[0038] The gate insulating layer 15 is intervened on the above-mentioned channel field, and the gate electrode 16 is formed. On the main front face of a silicon substrate 10, layer insulation layer 18a which consists of a silicon oxide etc. is formed so that this gate electrode 16 may be covered. Contact holes 11c and 11d are formed in this layer insulation layer 18a so that it may arrive at the impurity diffusion fields 14a and 14b. In contact hole 11c and 11d, the plug electrodes 17a and 17b which consist of W etc. are formed.
[0039] Layer insulation layer 18b is formed so that layer insulation layer 18a may be covered. A trench 23 is formed in this layer insulation layer 18b, and the substrate layer 19 which consists of TiN etc. is formed in this trench 23. The Cu wiring layer 20 is formed on this substrate layer 19, and the adhesion layer 21 is formed on this Cu wiring layer 20. And on this adhesion layer 21, the cap layer 22 which consists of TiWN is formed. On layer insulation layer 18b, layer insulation layer 18c is formed so that the cap layer 22 may be covered. In addition, although Cu wiring layer may be formed also in this layer insulation layer 18c, that illustration and explanation are omitted.

[0040] (Gestalt 2 of operation) Next, the gestalt 2 of implementation of this invention is explained using drawing 8 and drawing 9 . Drawing 8 is the sectional view showing the wiring structure in the gestalt 2 of implementation of this invention. Drawing 9 is the sectional view showing the modification of the wiring structure shown in drawing 8 .
[0041] With reference to drawing 8 , the reaction layer 8 is formed between the adhesion layer 5 and the Cu wiring layer 4 with the gestalt 2 of this operation. In this reaction layer 8, it is the layer formed of the counter diffusion of the element which constitutes the Cu wiring layer 4 and

the adhesion layer 5, and it becomes possible by forming such a reaction layer 8 to raise the connection resilience of the adhesion layer 5 and the Cu wiring layer 4 further from the case of the gestalt 1 of the above-mentioned operation. Consequently, it becomes possible from the case of the gestalt 1 of operation of the above [exfoliation of the cap layer 6] to control still more effectively.

[0042] As the formation approach of the above-mentioned reaction layer 8, when the adhesion layer 5 is constituted by Ti, it is 200 degrees C - about 400 degrees C in temperature, and can form by performing heat treatment for about 30 minutes within a vacuum or an inert gas ambient atmosphere.

[0043] Next, the modification of the wiring structure shown in drawing 8 is explained using drawing 9 . With reference to drawing 9 , the adhesion layer 5 located on the Cu wiring layer 4 is altogether changed into the reaction layer 8 in this modification by the above-mentioned heat treatment performed after forming the adhesion layer 5. Also in this case, it becomes possible from the case of the gestalt 1 of operation as well as the above-mentioned case to control exfoliation of the cap layer 6 still more effectively. In addition, in this modification, since it is necessary to change altogether into the reaction layer 8 the adhesion layer 5 located on the Cu wiring layer 4, the suitable heat treatment conditions according to the thickness of the adhesion layer 5 are chosen.

[0044] (Gestalt 3 of operation) Next, the gestalt 3 and modification of implementation of this invention are explained using drawing 10 - drawing 13 . Drawing 10 is the sectional view showing the wiring structure in the gestalt 3 of implementation of this invention.

[0045] With reference to drawing 10 , with the gestalt 3 of this operation, side-attachment-wall upper limit corner section 2a of a trench 2 is rounded off, and the cap layer 6 is formed so that it may extend on side-attachment-wall upper limit corner section 2a of such a trench 2 rounded off. As already pointed out as a trouble of the conventional example, the observation result of being easy to produce exfoliation in the periphery section of the cap layer 6 is obtained, and it is guessed that it is what a certain stress concentration tends to produce from this in the periphery section of the cap layer 6.

[0046] Then, the artificer of this application rounds off side-attachment-wall upper limit corner section 2a of a trench 2, and was made to make the periphery section of the cap layer 6 extend on this that the stress concentration in the periphery section of the cap layer 6 should be eased, as shown in drawing 10 . Thereby, the touch area of the periphery section of the cap layer 6 and an insulating layer 1 can be increased conventionally, and it is thought that it enables this to ease stress concentration. Consequently, it is thought that it becomes possible to control effectively exfoliation of the cap layer 6 which had become a problem in the conventional example.

[0047] Next, the manufacture approach of the wiring structure in the gestalt 3 of this operation is explained using drawing 11 - drawing 12 . Drawing 11 - drawing 12 are the sectional views showing the 1st process of the production process of the wiring structure in the gestalt 3 of this operation - the 2nd process.

[0048] After forming a trench 2 with reference to drawing 11 (a) through the same process as the case of the gestalt 1 of the above-mentioned operation, processing which rounds off side-attachment-wall upper limit corner section 2a of a trench 2 is performed. For example, when an insulating layer 1 is silicon oxide, light etching which used the fluoric acid system is performed. Thereby, side-attachment-wall upper limit corner section 2a of a trench 2 is rounded off according to an edge effect.

[0049] Although the enlarged drawing of side-attachment-wall upper limit corner section 2a of a trench 2 is shown in drawing 11 (b), as for side-attachment-wall upper limit corner section 2a, it is desirable to be constituted by the curved surface which has the predetermined radius of curvature r. And as for this radius of curvature r, it is desirable that it is about 2-20nm. That is because it is thought that spacing during adjoining wiring becomes large and trouble is caused to detailed-ization when it becomes difficult [implementation] very [radius of curvature r] when smaller than 2nm, and radius of curvature r exceeds 20nm. From this, in the range whose radius of curvature r is 2-20nm, it can realize and it is thought that it does not become a problem

mostly even if it faces detailed-ization.
[0050] In addition, although the case where the above-mentioned corner section 2a was constituted by the curved surface which has the fixed radius of curvature r was shown in drawing 11 (b), the curved surface which has different radius of curvature r may be put in a row. Moreover, if it sees microscopically, even if it cannot say that it is constituted by the curved surface, what sees on the whole and can be recognized as a curved surface is contained in the concept of the above-mentioned "curved surface."
[0051] Next, with reference to drawing 12 , the Cu wiring layer 4 and the substrate layer 3 are formed by the same approach as the case of the gestalt 1 of the above-mentioned operation, on these, the sputtering method etc. is used and TiWN layer 6a with a thickness of about 200nm is formed. And CMP processing is performed to TiWN layer 6a like the case of the gestalt 1 of the above-mentioned operation. This becomes possible to form the cap layer 6 in a trench 2, so that it may extend on side-attachment-wall upper limit corner section 2a of a trench 2, as shown in drawing 10 .
[0052] Next, the modification of the gestalt 3 of this operation is explained using drawing 13 . As shown in drawing 13 , in this modification, the adhesion layer 5 is formed between the cap layer 6 and the Cu wiring layer 4. It is thought that this becomes possible [controlling exfoliation of the cap layer 6 further] from the case of the gestalt 1 of the above-mentioned operation. In addition, also in this modification, a reaction layer 8 like [in the case of the gestalt 2 of the above-mentioned operation] may be formed.
[0053] As mentioned above, although the gestalt of implementation of this invention was explained, it should be thought that the gestalt of the operation indicated this time is [no] instantiation at points, and restrictive. The range of this invention is shown by the claim and it is meant that all modification in a claim, equal semantics, and within the limits is included.

[Translation done.]

* NOTICES *

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing the wiring structure of the semiconductor device in the gestalt 1 of implementation of this invention.
[Drawing 2] It is the sectional view showing the 1st process of the production process of the wiring structure shown in drawing 1 .
[Drawing 3] It is the sectional view showing the 2nd process of the production process of the wiring structure shown in drawing 1 .
[Drawing 4] It is the sectional view showing the 3rd process of the production process of the wiring structure shown in drawing 1 .
[Drawing 5] It is the sectional view showing the 4th process of the production process of the wiring structure shown in drawing 1 .
[Drawing 6] It is the sectional view showing the 5th process of the production process of the wiring structure shown in drawing 1 .
[Drawing 7] It is the fragmentary sectional view of the semiconductor device (DRAM) with which the wiring structure in the gestalt 1 of implementation of this invention was applied.
[Drawing 8] It is the sectional view showing the wiring structure of the semiconductor device in the gestalt 2 of implementation of this invention.
[Drawing 9] It is the sectional view showing the modification of the wiring structure shown in drawing 8 .
[Drawing 10] It is the sectional view showing the wiring structure of the semiconductor device in the gestalt 3 of implementation of this invention.
[Drawing 11] (a) is the sectional view showing the 1st process of the production process of the wiring structure shown in drawing 10 . (b) is drawing which expanded the side-attachment-wall upper limit corner section of the trench in (a).
[Drawing 12] It is the sectional view showing the 2nd process of the production process of the wiring structure shown in drawing 10 .
[Drawing 13] It is the sectional view showing the modification of the wiring structure shown in drawing 10 .
[Drawing 14] It is the sectional view showing an example of the wiring structure in the conventional semiconductor device.
[Drawing 15] It is the sectional view showing the 1st process of the production process of the wiring structure shown in drawing 14 .
[Drawing 16] It is the sectional view showing the 2nd process of the production process of the wiring structure shown in drawing 14 .
[Drawing 17] It is the sectional view showing the 3rd process of the production process of the wiring structure shown in drawing 14 .
[Drawing 18] It is the sectional view showing the 4th process of the production process of the wiring structure shown in drawing 14 .
[Description of Notations]
1, 12a, a 12b TiWN layer, 7 recess section, 8 reaction layers. An insulating layer, 2, 11a, 11b, 23 3 A trench, 2a side-attachment-wall upper limit corner section, 19 Substrate layer, 3a 4 A TiN

layer; 20 Cu wiring layer, 4a 5 Cu layer, 21 Adhesion layer, 5a 6 Ti layer, 22 A cap layer, 6a

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[Translation done.]

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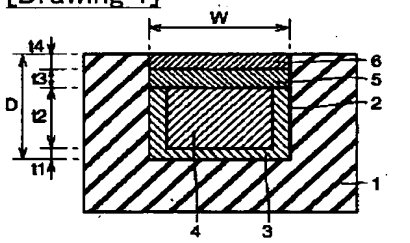
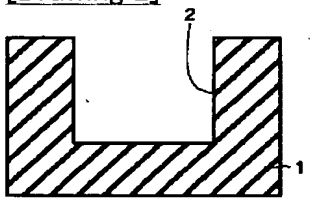
DRAWINGS

[Drawing 1]

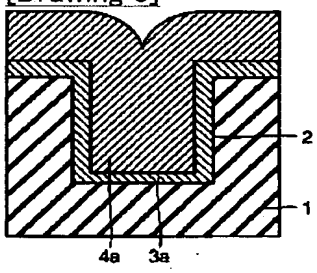


1：絶縁層　2：トレンチ　3：下地層
4：Cu配線層　5：密着層　6：キャップ層

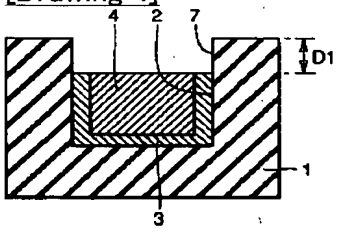
[Drawing 2]



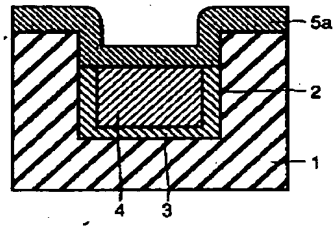
[Drawing 3]



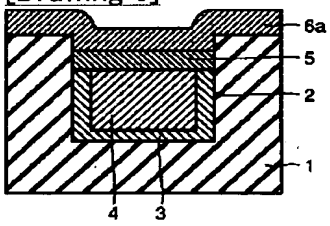
[Drawing 4]



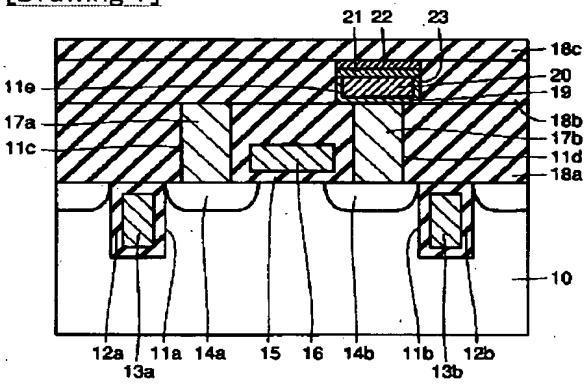
[Drawing 5]



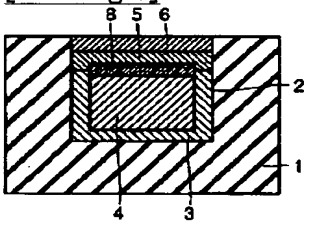
[Drawing 6]



[Drawing 7]

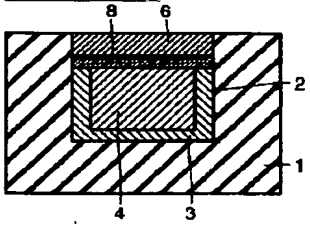


[Drawing 8]

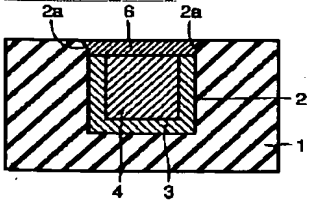


8：反応層

[Drawing 9]

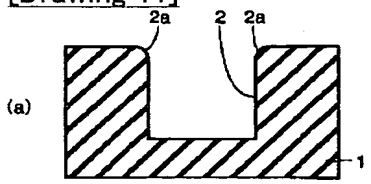


[Drawing 10]

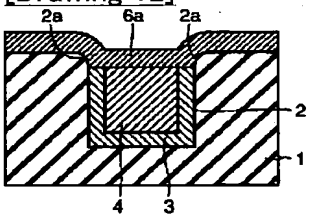


2a：側壁上端コーナ部

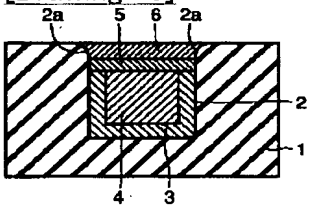
[Drawing 11]



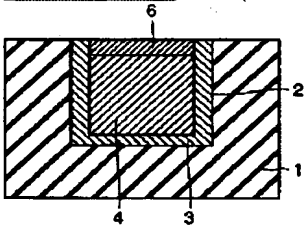
[Drawing 12]



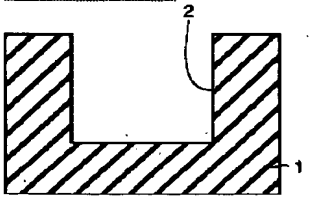
[Drawing 13]



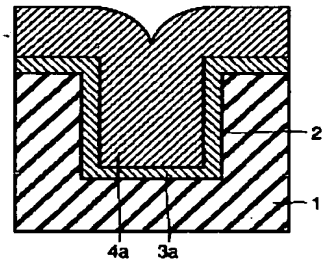
[Drawing 14]



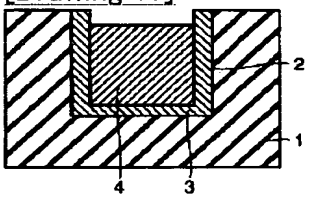
[Drawing 15]



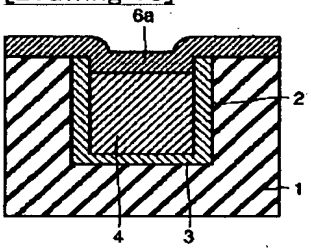
[Drawing 16]



[Drawing 17]



[Drawing 18]



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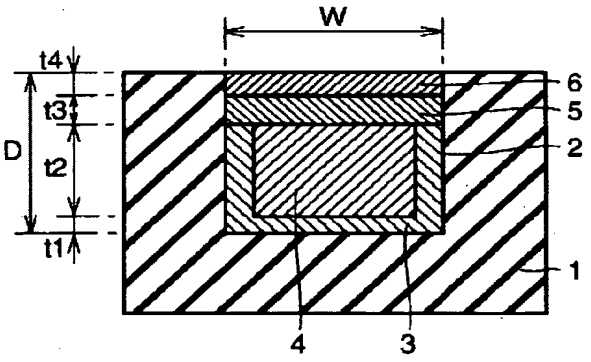
最終頁に続く

(54)【発明の名称】　半導体装置

(57)【要約】

【課題】　絶縁層に形成されたトレンチ内に埋込まれるＣｕ配線上に形成されるキャップ層の剥離を抑制する。

【解決手段】　絶縁層１に設けられたトレンチ２内に下地層３を介在してＣｕ配線層４を形成し、このＣｕ配線層４上に密着層５を形成する。この密着層５上にキャップ層６を形成する。



１：絶縁層　２：トレンチ　３：下地層
４：Cu配線層　５：密着層　６：キャップ層

【特許請求の範囲】
【請求項１】　トレンチが形成された絶縁層と、
前記トレンチ内に下地層を介在して埋込まれＣｕを含む材質により構成される配線層と、
前記配線層を覆うように前記トレンチ内に形成された密着層と、
前記密着層を覆うように前記トレンチ内に形成されたキャップ層と、を備えた、半導体装置。
【請求項２】　前記密着層は、前記配線層との密着強度が前記配線層と前記キャップ層との密着強度よりも大きく、かつ酸化物の成長速度が前記配線層におけるそれよりも小さい材質により構成される、請求項１に記載の半導体装置。
【請求項３】　前記キャップ層と前記配線層との間に、前記密着層と前記配線層とを反応させることにより反応層を形成した、請求項１または２に記載の半導体装置。
【請求項４】　前記配線層上に位置する前記密着層がすべて前記反応層に変換された、請求項３に記載の半導体装置。
【請求項５】　トレンチが形成された絶縁層と、
前記トレンチ内に下地層を介在して埋込まれＣｕを含む材質により構成される配線層とを備え、
前記トレンチの側壁上端コーナ部には、該コーナ部を丸める処理が施され、
前記配線層を覆うように前記トレンチ内にキャップ層が形成され、
前記キャップ層の周縁部は、前記コーナ部を丸める処理が施されることにより丸められた前記トレンチの側壁上端コーナ部上に延在する、半導体装置。
【請求項６】　前記トレンチの側壁上端コーナ部は、２～２０ｎｍの曲率半径を有する曲面により構成される、請求項５に記載の半導体装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は、半導体装置に関し、特に、絶縁層に形成されたトレンチ内に埋込まれ、Ｃｕを含む材質により構成される配線層を有する半導体装置に関するものである。
【０００２】
【従来の技術】半導体装置の高集積化および高速化に対する要求はますます高まりつつあり、このような高集積化および高速化に対応するため、配線材料についてもさまざまな検討がなされている。特に、配線幅が０．１５μｍ程度以降の世代では、配線材料として使用可能なものが極めて限定されてくるものと考えられる。このような材料の中で、近年、Ｃｕを配線材料として用いることが提案されている。
【０００３】図１４には、Ｃｕを配線材料として使用する場合の配線構造の一例が示されている。この図１４に示される配線構造は、いわゆる「ダマシン方式」と呼ばれる方式を用いた配線プロセスにより形成されたものである。ダマシン方式については、たとえば、月刊Semiconductor World １９９５．１２「ダマシン方式を用いた配線プロセス」等に記載されている。
【０００４】図１４に示されるように、絶縁層１にはトレンチ２が形成されており、このトレンチ２内に下地層３を介在してＣｕ配線層４が形成される。このＣｕ配線層４の上面を覆うようにキャップ層６が形成されている。このキャップ層６は、たとえばＴｉＷＮ等により構成され、Ｃｕ配線層４の上面の酸化を抑制する機能を有する。このようなキャップ層６を有することにより、Ｃｕ配線層４の上面の酸化が効果的に抑制され、Ｃｕ配線層４の抵抗上昇等の特性劣化を効果的に抑制することが可能となる。
【０００５】このようにキャップ層６を形成することについては、たとえば、信学技報TECHNICAL REPORT OF IEICE. ＳＤＭ９６－１６９（１９９６－１２）「ＴｉＷＮでキャップしたダマシンＣｕ配線」等に記載されている。
【０００６】次に、図１５～図１８を用いて、図１４に示される配線構造の製造方法について説明する。図１５～図１８は、図１４に示される配線構造の製造工程の第１工程～第４工程を示す断面図である。
【０００７】図１５を参照して、写真製版技術およびエッチング技術等を用いて、絶縁層１にトレンチ２を形成する。次に、図１６に示されるように、ＣＶＤ（Chemical Vapor Deposition）法等を用いてＴｉＮ層３ａを形成し、このＴｉＮ層３ａ上にスパッタリング法などを用いてＣｕ層４ａを形成する。
【０００８】次に、上記のＣｕ層４ａとＴｉＮ層３ａとにＣＭＰ（Chemical Mechanical Polishing）処理を施す。それにより、絶縁層１の表面を露出させるとともにトレンチ２内にのみＣｕ層を残す。その結果、図１７に示されるように、トレンチ２内に下地層３とＣｕ配線層４とがそれぞれ形成される。
【０００９】次に、図１８に示されるように、スパッタリング法などを用いて、ＴｉＷＮ層６ａを形成する。そして、このＴｉＷＮ層６ａにＣＭＰ処理を施す。以上の工程を経て、図１４に示される配線構造が得られることとなる。
【００１０】
【発明が解決しようとする課題】上記のようにキャップ層６ａを形成することによりＣｕ配線層４の上面の酸化を抑制することが可能となるが、本願の発明者が図１４に示される配線構造を試作したところ、上記のキャップ層６とＣｕ配線層４との界面で剥離が生じる場合があることを確認した。この剥離の１つの要因として、Ｃｕ配線層４とキャップ層６との密着強度が弱いということが考えられる。また、本願の発明者は、上記の剥離が、キャップ層６の周縁部において生じやすいことをも確認し

た。このことより、キャップ層６の周縁部において何らかの応力が集中し、この応力集中も上記の剥離の一因となり得るものと考えられる。

【００１１】キャップ層６とＣｕ配線層４との界面において上記のような剥離が生じることにより、Ｃｕ配線層４の上面が酸化され、Ｃｕ配線層４の抵抗上昇等の特性劣化が懸念される。そして、このようなＣｕ配線層４の特性劣化により、歩留りの低下や配線寿命の低下を招くこととなる。

【００１２】この発明は、上記のような課題を解決するためになされたものである。この発明の目的は、Ｃｕ配線層４の表面からの剥離を抑制することにある。

【００１３】

【課題を解決するための手段】この発明に係る半導体装置は、１つの局面では、絶縁層と、配線層と、密着層と、キャップ層とを備える。絶縁層にはトレンチが形成され、このトレンチ内に下地層を介在して配線層が埋込まれる。この配線層は、Ｃｕを含む材質により構成される。密着層は、配線層を覆うようにトレンチ内に形成され、キャップ層は、密着層を覆うようにトレンチ内に形成される。ここで、上記の下地層は、絶縁層の中への配線層材料の拡散防止機能および配線層と絶縁層との密着層としての機能を有する。また、密着層は、配線層とキャップ層との双方との密着強度が大きく、両者を強固に接続する機能を有する。また、キャップ層は、耐酸化性を有し、配線層が酸化されるのを抑制する機能を有する。

【００１４】なお、上記の密着層は、好ましくは、キャップ層との密着強度が配線層とキャップ層との密着強度よりも大きく、かつ酸化物の成長速度が配線層におけるそれよりも小さい材質により構成される。

【００１５】また、上記のキャップ層と配線層との間に、密着層と配線層とを反応させることにより反応層を形成することが好ましい。

【００１６】また、上記のように反応層を形成する場合には、配線層上に位置する密着層をすべて反応層に変換してもよい。

【００１７】この発明に係る半導体装置は、他の局面では、絶縁層と、配線層と、キャップ層とを備える。絶縁層にはトレンチが形成され、このトレンチ内に下地層を介在して配線層が埋込まれる。この配線層は、Ｃｕを含む材質により構成される。キャップ層は、配線層を覆うようにトレンチ内に形成される。そして、トレンチの側壁上端コーナ部には、このコーナ部を丸める処理が施される。たとえば、上記の絶縁層がシリコン酸化膜により構成される場合には、トレンチが形成された後の絶縁層に、フッ酸系を用いたライトエッチング処理を施す。このような処理が施されることによりトレンチ側壁上端コーナ部は丸められ、この丸められたトレンチの側壁上端コーナ部上に、上記のキャップ層の周縁部が延在する。

【００１８】なお、上記のトレンチの側壁上端コーナ部は、２～２０ｎｍの曲率半径を有する曲面により構成されることが好ましい。このとき、上記のように２～２０ｎｍの範囲内のものであれば、異なる曲率半径を有する曲面を連ねることによりトレンチの側壁上端コーナ部が構成されてもよい。

【００１９】

【発明の実施の形態】以下、図１～図１１を用いて、この発明の実施の形態について説明する。

【００２０】（実施の形態１）まず、図１～図７を用いて、この発明の実施の形態１について説明する。図１は、この発明の実施の形態１における配線構造を示す断面図である。

【００２１】図１を参照して、シリコン酸化膜などからなる絶縁層１にはトレンチ２が形成されている。トレンチ２の開口幅Ｗは、たとえば０．１８μｍ程度であり、トレンチ２の深さＤは０．３μｍ程度である。なお、トレンチ２のアスペクト比は１～１．５程度であってもよい。

【００２２】トレンチ２内には、たとえばＴｉＮなどからなる下地層３が形成される。この下地層３の厚みｔ１は、たとえば、１０ｎｍ程度である。この下地層３上にはＣｕ配線層４が形成される。このＣｕ配線層４の厚みｔ２は、たとえば２００ｎｍ程度である。なお、Ｃｕ配線層４の代わりにＣｕＺｒ，ＣｕＴｉ，ＣｕＡｌ等を使用することも可能である。

【００２３】Ｃｕ配線層４および下地層３を覆うように密着層５が形成される。この密着層５は、密着層５上に形成されるキャップ層６とＣｕ配線層４との密着強度を高めるべく形成されるものであり、密着層５とＣｕ配線層４との密着強度がＣｕ配線層４とキャップ層６の密着強度よりも大きく、かつ酸化物の成長速度がＣｕ配線層４におけるそれよりも小さい材質により構成されることが好ましい。それにより、Ｃｕ配線層４とキャップ層６との接続強度を従来例よりも高めることが可能となるとともに、Ｃｕ配線層４の上面が酸化されることをも効果的に抑制することが可能となる。

【００２４】上記の密着層５の材質としては、Ｔｉ，ＴｉＮ，Ｃｒ，Ａｌ，ＡｌＣｕ，ＡｌＳｉＣｕ等を挙げることができる。また、この密着層５の厚みｔ３は、３～５０ｎｍ程度であることが好ましい。このような厚みとすることにより、上述のような効果が期待できる。

【００２５】キャップ層６は、この場合であれば、ＴｉＷＮにより構成される。このキャップ層６は、図１に示されるように、密着層５を覆うようにトレンチ２内に埋込まれる。また、このキャップ層６の厚みｔ４は、たとえば３０ｎｍ～７７ｎｍ程度である。このような厚みとすることにより、キャップ層６の耐酸化性を確保することが可能となる。

【００２６】上記のような密着層５を形成することによ

り、キャップ層６の剥離を効果的に抑制することが可能となるものと考えられる。本願の発明者は、このことを立証すべく、密着層５を形成した場合にキャップ層６の剥離が生ずるか否かの評価を行なった。その評価結果が表１に示されている。なお、表１では、密着層５としてＴｉ層を形成した場合が示されている。

【００２７】

【表１】

構造	CMP時のTiWN層に対するストレス	
	ストレス大(研磨レート大:約400nm/min.)	ストレス小(研磨レート小:約100nm/min.)
TiN/Cu/TiWN	配線エッジ部から剥離	配線エッジ部で部分的な剥離有り
TiN/Cu/Ti/TiWN	剥離無し	剥離無し
TiN/Cu/Ti/TiWN(熱処理有り)	剥離無し	剥離無し

【００２８】表１に示されるように、密着層５として機能するＴｉ層を形成した場合には、ＣＭＰ後のキャップ層（ＴｉＷＮ層）に対するストレスの大小にかかわらず剥離が生じていないのがわかる。このことより、密着層５を形成することにより、キャップ層６の剥離を効果的に抑制することが可能となるものと考えられる。なお、密着層５としてＴｉ層以外の上記材質を用いた場合にも同様の結果が得られるものと推察される。また、表１には、密着層５を形成した後に熱処理を施したものについても記載されているが、これについては後述する。

【００２９】次に、図２～図６を用いて、図１に示される配線構造の製造方法について説明する。図２～図６は、図１に示される配線構造の製造工程の第１工程～第５工程を示す断面図である。

【００３０】図２を参照して、たとえば写真製版技術とドライエッチング技術とを用いて、トレンチ２を形成する。このトレンチ２の寸法については上述したとおりである。

【００３１】次に、たとえばＣＶＤ法等を用いて、トレンチ２内から絶縁層１上に延在するように１０ｎｍ程度の厚みにＴｉＮ層３ａを形成する。このＴｉＮ層３ａ上に、ＣＶＤ法あるいはスパッタリング法を用いて、４００ｎｍ程度の厚みのＣｕ層４ａを形成する。

【００３２】次に、上記のＣｕ層４ａとＴｉＮ層３ａとにＣＭＰ処理を施す。このＣＭＰ処理は、たとえばアルミナベースのスラリーを用いて行なってもよい。そして、絶縁層１の主表面が露出するまでＣＭＰ処理を行なう。その結果、図４に示されるように、Ｃｕ配線層４と下地層３とが形成されるとともに、これらの上にリセス部７が形成される。このリセス部７の深さＤ１は、後の工程で形成される密着層５とキャップ層６との厚みの和となるように選定され、この場合であれば、たとえば８０ｎｍ程度である。なお、リセス部７の深さＤ１は、５０～８０ｎｍ程度と比較的小さい値に設定されることが好ましい。それにより、Ｃｕ配線層４の断面積の減少を抑制でき、配線抵抗の上昇を抑制できる。

【００３３】次に、図５に示されるように、たとえばスパッタリング法等を用いて、２００ｎｍ程度の厚みにＴｉ層５ａを形成する。そして、このＴｉ層５ａにＣＭＰ処理を施す。

【００３４】それにより、図６に示されるように、トレンチ２内に埋込まれるように密着層５を形成することが可能となる。その後、さらにスパッタリング法等を用いて、ＴｉＷＮ層６ａを２００ｎｍ程度の厚みに形成する。そして、このＴｉＷＮ層６ａにもＣＭＰ処理を施す。この場合にも、アルミナベースのスラリーを用いたＣＭＰ処理を行なってもよい。以上の工程を経て、図１に示される配線構造が得られることとなる。

【００３５】なお、上記のＴｉ層５ａとＴｉＷＮ層６ａとを順次形成し、これらの積層構造にＣＭＰ処理を施すものであってもよい。

【００３６】次に、図７を用いて、本実施の形態１における配線構造の適用例について説明する。図７は、上記の実施の形態１における配線構造が適用された半導体装置の一例を示す断面図である。具体的には、上記の実施の形態１の配線構造が適用されたＤＲＡＭ（Dynamic Random Access Memory）の一部が図７に示されている。

【００３７】図７を参照して、シリコン基板１０の主表面にはチャネル領域を規定するように不純物拡散領域１４ａ，１４ｂが形成される。この不純物拡散領域１４ａ，１４ｂの両側にはトレンチ１１ａ，１１ｂが形成される。トレンチ１１ａ，１１ｂ内には絶縁層１２ａ，１２ｂを介在してポリシリコン層１３ａ，１３ｂがそれぞれ形成される。

【００３８】上記のチャネル領域上にはゲート絶縁層１５を介在してゲート電極１６が形成される。このゲート電極１６を覆うようにシリコン基板１０の主表面上には、シリコン酸化物などからなる層間絶縁層１８ａが形成される。この層間絶縁層１８ａには、不純物拡散領域１４ａ，１４ｂに到達するようにコンタクトホール１１ｃ，１１ｄが形成される。コンタクトホール１１ｃ，１１ｄ内にはＷなどからなるプラグ電極１７ａ，１７ｂが形成される。

【００３９】層間絶縁層１８ａを覆うように層間絶縁層１８ｂが形成される。この層間絶縁層１８ｂにはトレンチ２３が形成され、このトレンチ２３内にはＴｉＮ等からなる下地層１９が形成される。この下地層１９上にはＣｕ配線層２０が形成され、このＣｕ配線層２０上には密着層２１が形成される。そして、この密着層２１上には、ＴｉＷＮからなるキャップ層２２が形成される。キ

ャップ層２２を覆うように層間絶縁層１８ｂ上には層間絶縁層１８ｃが形成される。なお、この層間絶縁層１８ｃ内にもＣｕ配線層が形成されてもよいが、その図示と説明は省略する。

【００４０】（実施の形態２）次に、図８と図９を用いて、この発明の実施の形態２について説明する。図８は、この発明の実施の形態２における配線構造を示す断面図である。図９は、図８に示される配線構造の変形例を示す断面図である。

【００４１】図８を参照して、本実施の形態２では、密着層５とＣｕ配線層４との間に反応層８が形成されている。この反応層８とは、Ｃｕ配線層４と密着層５とを構成する元素の相互拡散により形成された層であり、このような反応層８を形成することにより、上記の実施の形態１の場合よりもさらに密着層５とＣｕ配線層４との接続強度を高めることが可能となる。その結果、キャップ層６の剥離を上記の実施の形態１の場合よりもさらに効果的に抑制することが可能となる。

【００４２】上記の反応層８の形成方法としては、密着層５がたとえばＴｉにより構成される場合には、２００℃～４００℃程度の温度で、真空あるいは不活性ガス雰囲気内での３０分程度の熱処理を施すことにより形成可能である。

【００４３】次に、図９を用いて、図８に示される配線構造の変形例について説明する。図９を参照して、本変形例では、密着層５を形成した後に施される上記の熱処理により、Ｃｕ配線層４上に位置する密着層５がすべて反応層８に変換されている。この場合にも、上記の場合と同様に、実施の形態１の場合よりもさらに効果的にキャップ層６の剥離を抑制することが可能となる。なお、本変形例では、Ｃｕ配線層４上に位置する密着層５をすべて反応層８に変換する必要があるため、密着層５の厚みに応じた適切な熱処理条件が選択される。

【００４４】（実施の形態３）次に、図１０～図１３を用いて、この発明の実施の形態３とその変形例とについて説明する。図１０は、この発明の実施の形態３における配線構造を示す断面図である。

【００４５】図１０を参照して、本実施の形態３では、トレンチ２の側壁上端コーナ部２ａが丸められ、このような丸められたトレンチ２の側壁上端コーナ部２ａ上に延在するようにキャップ層６が形成されている。従来例の問題点として既に指摘したように、キャップ層６の周縁部において剥離が生じやすいという観察結果が得られており、このことからキャップ層６の周縁部において何らかの応力集中が生じやすいのではないかと推察される。

【００４６】そこで、本願の発明者は、キャップ層６の周縁部での応力集中を緩和すべく、図１０に示されるように、トレンチ２の側壁上端コーナ部２ａを丸め、この上にキャップ層６の周縁部を延在させるようにした。それにより、キャップ層６の周縁部と絶縁層１との接触面積を従来よりも増大させることができ、それにより応力集中を緩和することが可能となると考えられる。その結果、従来例で問題となっていたキャップ層６の剥離を効果的に抑制することが可能となると考えられる。

【００４７】次に、図１１～図１２を用いて、本実施の形態３における配線構造の製造方法について説明する。図１１～図１２は、本実施の形態３における配線構造の製造工程の第１工程～第２工程を示す断面図である。

【００４８】図１１（ａ）を参照して、上記の実施の形態１の場合と同様の工程を経てトレンチ２を形成した後、トレンチ２の側壁上端コーナ部２ａを丸める処理を施す。たとえば、絶縁層１がシリコン酸化膜の場合には、フッ酸系を用いたライトエッチングを行なう。それにより、トレンチ２の側壁上端コーナ部２ａがエッジ効果により丸められる。

【００４９】図１１（ｂ）には、トレンチ２の側壁上端コーナ部２ａの拡大図が示されているが、側壁上端コーナ部２ａは、所定の曲率半径ｒを有する曲面により構成されることが好ましい。そして、この曲率半径ｒは、２～２０ｎｍ程度であることが好ましい。それは、曲率半径ｒが２ｎｍより小さい場合には実現が極めて困難となり、曲率半径ｒが２０ｎｍを超えた場合には隣接する配線間の間隔が大きくなり微細化に支障をきたすと考えられるからである。このことより、曲率半径ｒが２～２０ｎｍの範囲では実現可能であり、微細化に際してもほぼ問題とならないと考えられる。

【００５０】なお、図１１（ｂ）には、一定の曲率半径ｒを有する曲面により上記コーナ部２ａが構成された場合について示したが、異なる曲率半径ｒを有する曲面を連ねたものであってもよい。また、微視的にみれば曲面により構成されているとはいえなくても、全体的にみて曲面として認識できるものも上記の「曲面」の概念に含まれる。

【００５１】次に、図１２を参照して、上記の実施の形態１の場合と同様の方法でＣｕ配線層４と下地層３とを形成し、これらの上に、スパッタリング法などを用いて、２００ｎｍ程度の厚みのＴｉＷＮ層６ａを形成する。そして、上記の実施の形態１の場合と同様に、ＴｉＷＮ層６ａにＣＭＰ処理を施す。それにより、図.１０に示されるように、トレンチ２内に、トレンチ２の側壁上端コーナ部２ａ上に延在するようにキャップ層６を形成することが可能となる。

【００５２】次に、図１３を用いて、本実施の形態３の変形例について説明する。図１３に示されるように、本変形例では、キャップ層６とＣｕ配線層４との間に密着層５が形成されている。それにより、上記の実施の形態１の場合よりもさらにキャップ層６の剥離を抑制することが可能となると考えられる。なお、本変形例においても、上記の実施の形態２の場合のような反応層８を形成

してもよい。

【００５３】以上のように、この発明の実施の形態について説明を行なったが、今回開示された実施の形態はすべての点で例示であって制限的なものではないと考えられるべきである。本発明の範囲は特許請求の範囲によって示され、特許請求の範囲と均等の意味および範囲内でのすべての変更が含まれることが意図される。

【００５４】

【発明の効果】以上説明したように、この発明に係る半導体装置の１つの局面では、配線層上に密着層が形成され、この密着層上にキャップ層が形成される。密着層としては、キャップ層および配線層との密着強度が大きい材質が選択されるので、密着層の存在によりキャップ層の剥離を効果的に抑制することが可能となる。それにより、キャップ層の剥離に起因して配線層の上面が酸化されることを効果的に抑制することが可能となり、配線欠陥の発生を効果的に抑制することが可能となる。その結果、従来よりも歩留りを向上させることが可能となるとともに、配線寿命をも向上させることが可能となる。

【００５５】なお、上記の密着層が、該密着層と配線層との密着強度が配線層とキャップ層との密着強度よりも大きく、かつ酸化物の成長速度が配線層におけるそれよりも小さい材質により構成された場合には、キャップ層の剥離を効果的に抑制できるばかりでなく、かかる密着層の存在により配線層の上面が酸化されることをも抑制することが可能となる。

【００５６】また、キャップ層と配線層との間に、密着層と配線層とを反応させることによる反応層を形成した場合には、この反応層が配線層の材料と密着層の材料との相互拡散により形成されることから、上記の場合よりもさらに効果的にキャップ層の剥離を抑制することが可能となる。

【００５７】また、上記の密着層はすべて反応層に変換されてもよく、この場合にも、密着層と配線層との間に反応層が形成された場合と同様に、効果的にキャップ層の剥離を抑制することが可能となる。

【００５８】この発明に係る半導体装置の他の局面では、絶縁層に形成されたトレンチの側壁上端コーナ部を丸めている。そして、このように丸められた側壁上端コーナ部上にキャップ層を延在させている。それにより、キャップ層の周縁部と絶縁層との接触面積を、従来より増大させることが可能となる。それにより、従来例において懸念されていたキャップ層の周縁部における応力集中を緩和でき、従来例よりもキャップ層の剥離を抑制することが可能となる。

【００５９】なお、上記の側壁上端コーナ部は２～２０ｎｍ程度の曲率半径を有する曲面により構成されることが好ましく、曲率半径をこのような範囲内とすることにより、容易に実現可能でありかつ半導体装置の微細化に際しても支障をきたさないという効果が得られる。

【図面の簡単な説明】

【図１】　この発明の実施の形態１における半導体装置の配線構造を示す断面図である。

【図２】　図１に示される配線構造の製造工程の第１工程を示す断面図である。

【図３】　図１に示される配線構造の製造工程の第２工程を示す断面図である。

【図４】　図１に示される配線構造の製造工程の第３工程を示す断面図である。

【図５】　図１に示される配線構造の製造工程の第４工程を示す断面図である。

【図６】　図１に示される配線構造の製造工程の第５工程を示す断面図である。

【図７】　この発明の実施の形態１における配線構造が適用された半導体装置（ＤＲＡＭ）の部分断面図である。

【図８】　この発明の実施の形態２における半導体装置の配線構造を示す断面図である。

【図９】　図８に示される配線構造の変形例を示す断面図である。

【図１０】　この発明の実施の形態３における半導体装置の配線構造を示す断面図である。

【図１１】　（ａ）は図１０に示される配線構造の製造工程の第１工程を示す断面図である。（ｂ）は（ａ）におけるトレンチの側壁上端コーナ部を拡大した図である。

【図１２】　図１０に示される配線構造の製造工程の第２工程を示す断面図である。

【図１３】　図１０に示される配線構造の変形例を示す断面図である。

【図１４】　従来の半導体装置における配線構造の一例を示す断面図である。

【図１５】　図１４に示される配線構造の製造工程の第１工程を示す断面図である。

【図１６】　図１４に示される配線構造の製造工程の第２工程を示す断面図である。

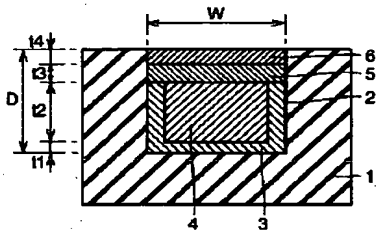
【図１７】　図１４に示される配線構造の製造工程の第３工程を示す断面図である。

【図１８】　図１４に示される配線構造の製造工程の第４工程を示す断面図である。

【符号の説明】

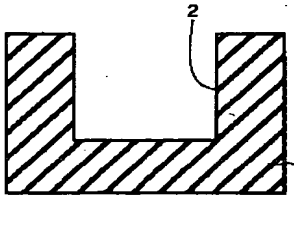
１，１２ａ，１２ｂ　絶縁層、２，１１ａ，１１ｂ，２３　トレンチ、２ａ側壁上端コーナ部、３，１９　下地層、３ａ　ＴｉＮ層、４，２０　Ｃｕ配線層、４ａ　Ｃｕ層、５，２１　密着層、５ａ　Ｔｉ層、６，２２　キャップ層、６ａ　ＴｉＷＮ層、７　リセス部、８　反応層。

【図１】

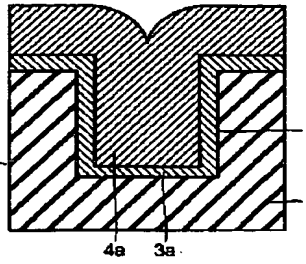


1：絶縁層　2：トレンチ　3：下地層
4：Cu配線層　5：密着層　6：キャップ層

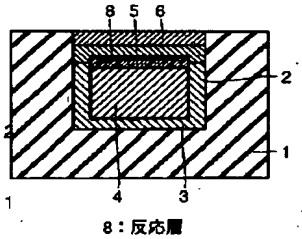
【図２】



【図３】

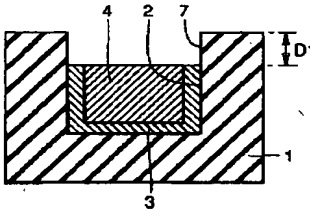


【図８】

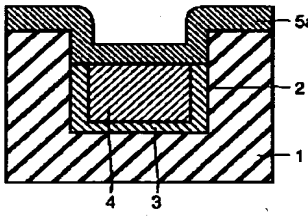


8：反応層

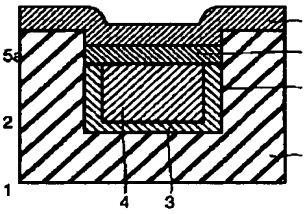
【図４】



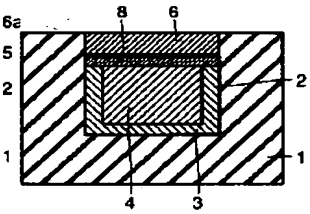
【図５】



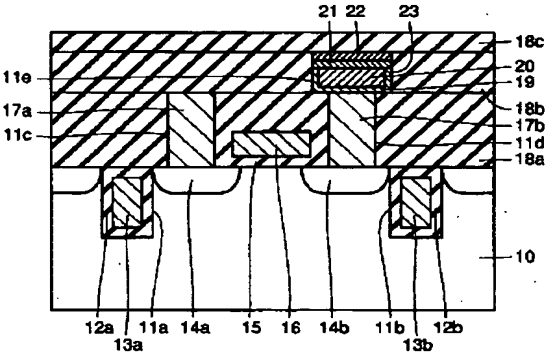
【図６】



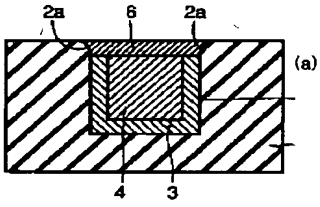
【図９】



【図７】

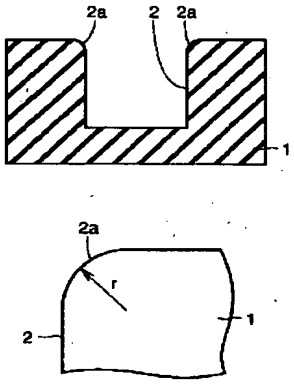


【図１０】

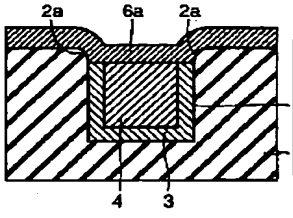


2a：側壁上端コーナ部

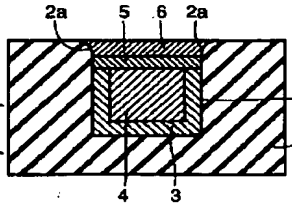
【図１１】



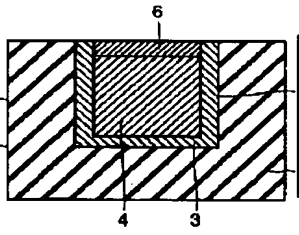
【図１２】



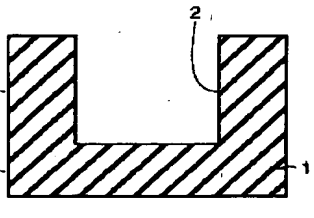
【図１３】



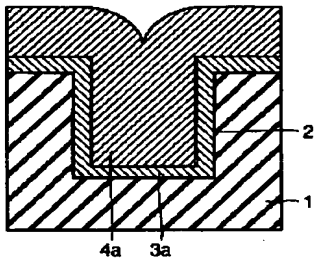
【図１４】



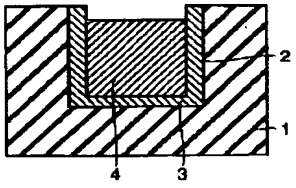
【図１５】



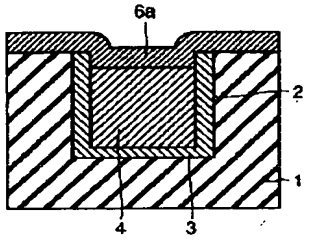
【図１６】



【図１７】



【図１８】



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